Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application. All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1-15 remain.

WHAT IS CLAIMED IS:

1. (Original) A programmable digital filter integrated circuit, comprising:

a. a bus;

b. a processor, connected to said bus, for performing digital filtering on digital signals; and

c. a programmable interface, connected to said bus, for selectively receiving digital signals having different properties for filtering by said processor

2. (Original) The integrated circuit of claim 1 in which said properties include data rate.

3. (Original) The integrated circuit of claim 1 in which said properties include algorithm by which said digital signals were encoded.

4. (Original) The integrated circuit of claim 1 in which said programmable interface includes:

a. a data input port;

b. a plurality of input latches connected to said input port;

c. a multiplexor, having a plurality of inputs, each receiving a respective output from an input latch; for selecting an input latch to be connected to a multiplexor output.

5. (Original) The integrated circuit of claim 4 in which the output of said multiplexor is connected to at least one sinc filter.

6. (Original) The integrated circuit of claim 5 in which the output of said multiplexor is connected to two different sinc filters.

7. (Original) The integrated circuit of claim 6 in which said two different sinc filters can be selectively activated.

8. (Original) The integrated circuit of claim 6 in which one of said sinc filters is a 5th order decimate by 8 sinc filter.

9. (Original) The integrated circuit of claim 6 in which one of said sinc filters is a 6th order decimate by 2 sinc filter.

10. (Original) The integrated circuit of claim 5 in which the inputs to said two different sinc filters may be selectively connected to said multiplexor or to a test signal data source.

11. (Original) The integrated circuit of claim 4 in which the output of the multiplexor is connected to a first sinc filter and the output of the first sinc filter is connected to a programmable sinc filter.

12. (Original) The integrated circuit of claim 11 in which said programmable sinc filter comprises selectable combinations of a plurality of sinc filters.

13. (Original) The integrated circuit of claim 11 in which said plurality of sinc filters comprise two 4th order decimate by 2 sinc filters, a 5th order decimate by 2 sinc filter, a 6th order decimate by 2 sinc filter and a 4th order decimate by 3 sinc filter.

14. (Original) A method of designing an integrated circuit, comprising the steps of:

a. providing a bus;

b. providing a processor, connected to said bus, for performing digital filtering on digital signals; and

c. providing a programmable interface, connected to said bus, for selectively receiving digital signals having different properties for filtering by said processor.

15. (Original) A method of fabricating an integrated circuit, comprising the steps of:

a. providing a bus;

b. providing a processor, connected to said bus, for performing digital filtering on digital signals; and

c. providing a programmable interface, connected to said bus, for selectively receiving digital signals having different properties for filtering by said processor.